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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,934	12/23/2003	Jin Su Park	29936/39901	9005

4743 7590 05/02/2005

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/743,934	PARK, JIN SU
	Examiner	Art Unit
	Anh Q. Tran	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al (6,650,168).

Wang shows:

1. A data input/output buffer, comprising:

a plurality of switching elements (353, Fig. 5) and a plurality of logical elements (320-336 and core circuit),

wherein an NMOS transistor (ZN1 or ZN2) of a switching element driven according to a data signal inputted from a peripheral circuit or a logical element to which the data signal is inputted, of the plurality of the switching elements or the plurality of the logical elements, is a low voltage-driven NMOS transistor.

2. The data input/output buffer as claimed in claim 1, wherein a threshold voltage of the low voltage-driven NMOS transistor is OV (col. 6, lines 30-55).

3. Claims 1, 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Onishi (6,542,011)

Onishi shows:

1. A data input/output buffer, comprising:

a plurality of switching elements (41-43, Fig. 2) and a plurality of logical elements (20),

wherein an NMOS transistor (42-43) of a switching element driven according to a data signal inputted from a peripheral circuit or a logical element to which the data signal is inputted, of the plurality of the switching elements or the plurality of the logical elements, is a low voltage-driven NMOS transistor (col. 9, lines 1-3).

5. A data input/output buffer, comprising: a first logical element driven according to a data signal inputted from a peripheral circuit (through 7 to 8, Fig. 1), the first logical element having a PMOS transistor (41) and a low voltage-driven NMOS transistor (42-43); and a second logical element (44-45) for latching an output signal of the first logical element.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-4, 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Onishi (6,542,011).

2, 6. Onishi discloses the claimed invention except for 0V NMOS transistor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify NMOS transistor of Onishi having a threshold voltage of 0V, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

3, 7. The data input/output buffer as claimed in claim 2, further comprising a switching element (42) that is turned on according to an output enable signal (ACT) only when a data is outputted between the low voltage-driven NMOS transistor and a ground voltage terminal.

4, 8. The data input/output buffer as claimed in claim 3, wherein the switching element is an NMOS transistor.

Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takano (6,842,377) in view of Onishi (6,542,011).

9. Takano show semiconductor memory device, comprising:

a memory cell array (21, Fig. 2);

row decoder (22) for selecting a given page of the memory cell array according to a row address signal (6, Fig. 1);

a page buffer (42, Fig. 10) for storing data stored at the page selected by the row decoder; a column decoder (23) for generating a bit line select signal according to a column address signal (8, Fig. 1); a column multiplexer (96) for selecting and outputting any one of the data stored at the page buffer according to the bit line select signal; and

a data input/output buffer (9, Fig. 1) for storing the data selected by the column multiplexer and transferring the data to a data line. Takano discloses the claimed invention except for a device driven by the data is a low voltage-driven NMOS transistor. Onishi discloses a driver circuit for transfer data is a low voltage-driven NMOS transistor (42, Fig. 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the data input/output buffer of Takano with the driver circuit having a low voltage-driven NMOS transistor of Onishi, in order to reduce power consumption and improve the performance of the digital signal transfer circuit.

10. Takana and Onishi discloses the claimed invention except for 0V NMOS transistor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify NMOS transistor of Onishi having a threshold voltage of 0V, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

11. Onishi discloses a switching element (42) that is turned on according to an output enable signal (ACT) only when a data is outputted between the low voltage-driven NMOS transistor and a ground voltage terminal.

12. Onishi discloses the switching element is an NMOS transistor (42).

13. Onishi discloses a PMOS transistor (41), a low voltage-driven NMOS transistor (42) connected to the PMOS transistor, a switching element connected between the low voltage-driven NMOS transistor and a ground voltage terminal, wherein the switching element (43) is turned on only in a data output period and a latch unit (44, 45).

14. Onishi discloses the switching element is an NMOS transistor (43).

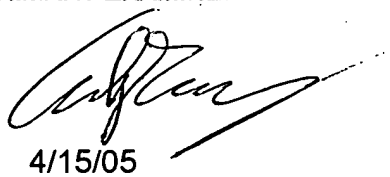
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER



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